NASA SP-5964 (01)

TECHNOLOGY UTILIZATION

ELECTRONIC CONTROL CIRCUITS

A COMPILATION

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Foreword

The National Aeronautics and Space Administration and the Atomic Energy Commission have established a Technology Utilization Program for the dissemination of information on technological developments which have potential utility outside the aerospace and nuclear communities. By encouraging multiple application of the results of their research and development, NASA and AEC earn for the public an increased return on the investment in aerospace and nuclear research and development programs.

This compilation is part of a series intended to provide such technical information. The circuits and modular subassemblies are only samples of many similar items that are available through the TU program. The enormous volume of information available in this fertile area is indicative of the important role that electronic control technology has played in the aerospace and nuclear programs.

In general, the compilation items are moderately complex and as such would appeal to the applications engineer. However, the rationale for the selection criteria was tailored so that the circuits would reflect fundamental design principles and applications, with an additional requirement for simplicity whenever possible.

Additional technical information on individual devices and techniques can be requested by circling the appropriate number on the Reader Service Card included in this compilation.

Unless otherwise stated, NASA and AEC contemplate no patent action on the technology described.

We appreciate comment by readers and welcome hearing about the relevance and utility of the information in this compilation.

Jeffrey T. Hamilton, *Director*
Technology Utilization Office
National Aeronautics and Space Administration

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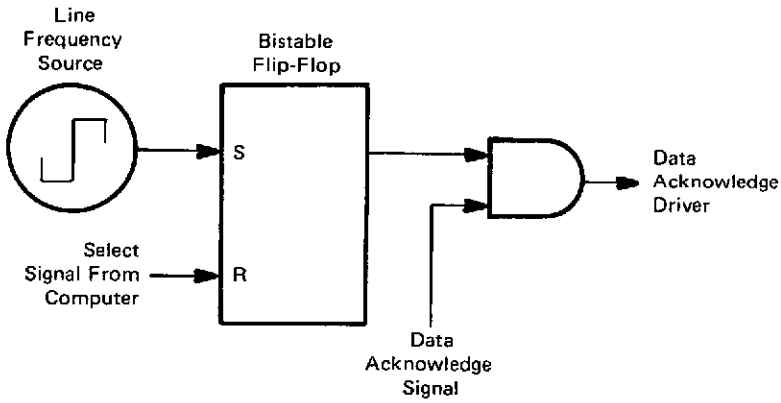
Contents

Electronic Control Circuits

DISPLAY SYNCHRONIZER ELIMINATES JITTER



Display Synchronizer

The addition of a logical AND gate to a computer-driven display circuit eliminates the jitter caused by power line pickup. The gate (see fig.) synchronizes the display with the power line frequency.

The AND gate is added to the display circuit which signals the computer that a data word has been received. This gate is controlled by a bi-stable flip-flop. The flip-flop is reset whenever the computer selects a device on the data channel; it is set by a line frequency pulse generator.

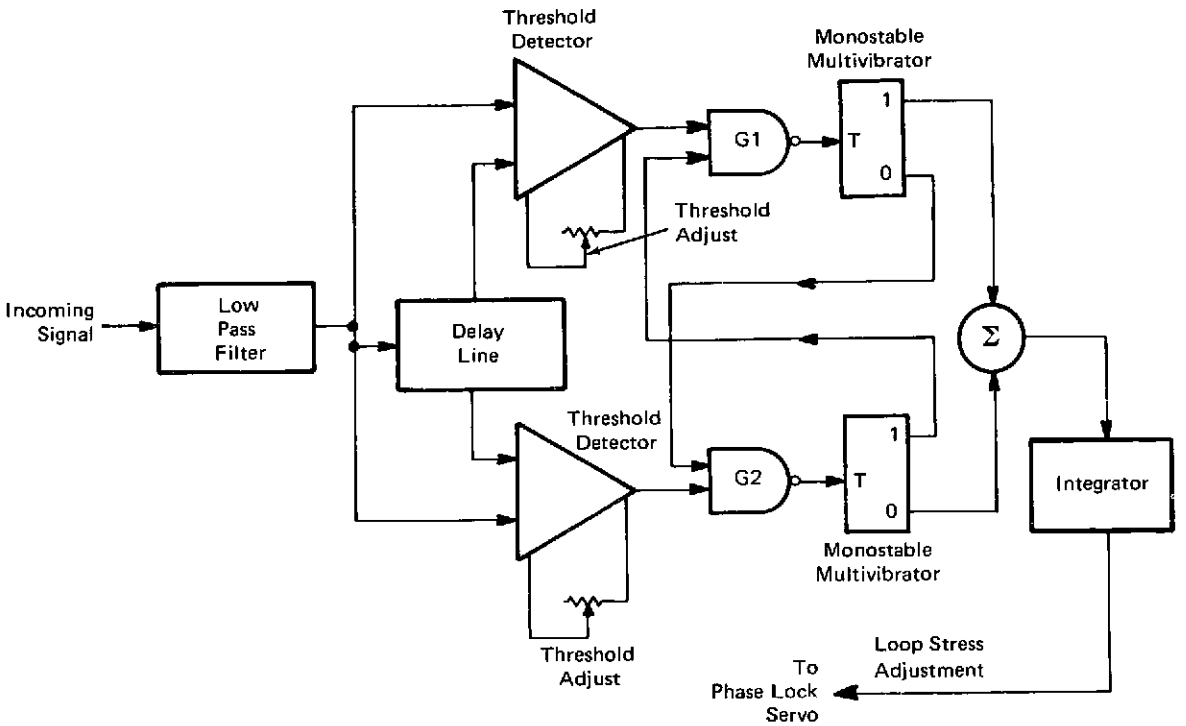
An important feature of this logic is that the computer can select the display unit at any time, set up the data channel, and go on to other tasks. Only the data channel portion of the computer is delayed by the wait to start the display at the proper time with respect to the line frequency.

Almost any multivibrator driven by an isolation transformer from the power line makes a suitable line frequency pulse generator.

Source: L. Linstrom
Goddard Space Flight Center
(GSC-11098)

No further documentation is available.

DELAY LINE CLICK DETECTOR: A CONCEPT



The noise suppressing advantages of frequency- and phase-modulated systems are sometimes diminished when the amount of radio frequency (RF) energy available at the receiving antenna is small. Under these conditions, Gaussian and random noises are rejected, but occasionally a noise spike is generated when the incoming signal shifts frequency and causes a rapid phase shift in the band pass of the receiver discriminator. This noise spike or click occurs abruptly and usually has a high amplitude which causes unsatisfactory signal reception.

Previous attempts to eliminate the clicks have centered around their detection and suppression by using amplitude-sensitive threshold circuits. Noise clicks exceeding a predetermined modulation amplitude would thus be detected. However, if the thresholds were set too low or too high, the signals reaching the output of the receiver would contain errors.

The delay line click detector (see fig.) relies on the use of a delay line that allows the incoming signal to be time displaced and compared against itself. Thus, if the incoming signal is clickless, the correlation on comparison will be zero. However, if a click is superimposed on the modulation, its duration time will be short enough so that the delayed comparison will show a positive or negative difference. The series of positive and negative difference signals are integrated and fed back to a phase lock servo loop in the demodulator portion of the receiver. The feedback is called a "loop stress adjustment".

As indicated, the delay line is used to delay the signal appearing at one side of each of a pair of threshold sensors by a fixed time interval T. A low-pass filter ahead of the threshold detectors and the delay line restricts the range of frequencies so that the delay T is a small fraction of the period of the highest frequency passed by the filter. However, the maximum differential level between the two inputs to each threshold detector is a function of the frequency of the modulation coming through the low-pass filter as well as any short term dissymmetry characteristic of a noise click.

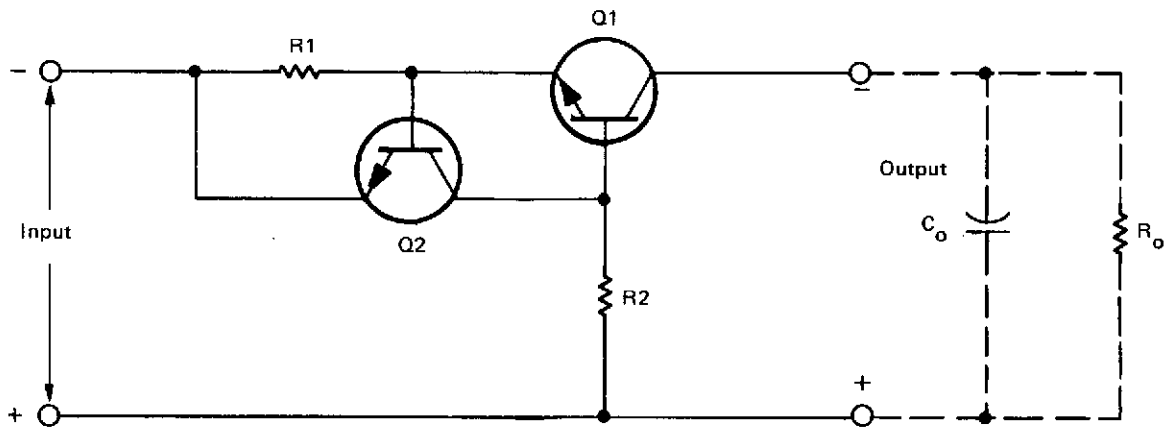
To avoid multiple triggering of a click event, a NAND gate follows each threshold detector and precedes each monostable multivibrator. Gates G1

and G2 inhibit the input to the untriggered multivibrator until the triggered multivibrator has completed its cycle. The multivibrators normalize the click widths so that they are wide enough to be integrated. The detected signals are then integrated to determine the numerical imbalance between the positive and negative noise clicks.

Source: J. R. Pousson of
TRW, Inc.
under contract to
Johnson Space Center
(MSC-13240)

No further documentation is available.

CIRCUIT LIMITER



The primary purpose of this circuit (see fig.) is to limit current surges during power turn-on of DC sources. The circuit has application in systems where current limiting is required during power sequencing.

When a voltage step function is applied at the input terminals, current builds up through the Q1 collector, and the voltage across R1 increases until the base-to-emitter state of Q2 becomes forward biased at approximately 0.5 volts. As transistor Q2 turns on, the base current to Q1 is reduced, and Q1 tends to turn off, thus limiting the current that is supplied to the load to approximately

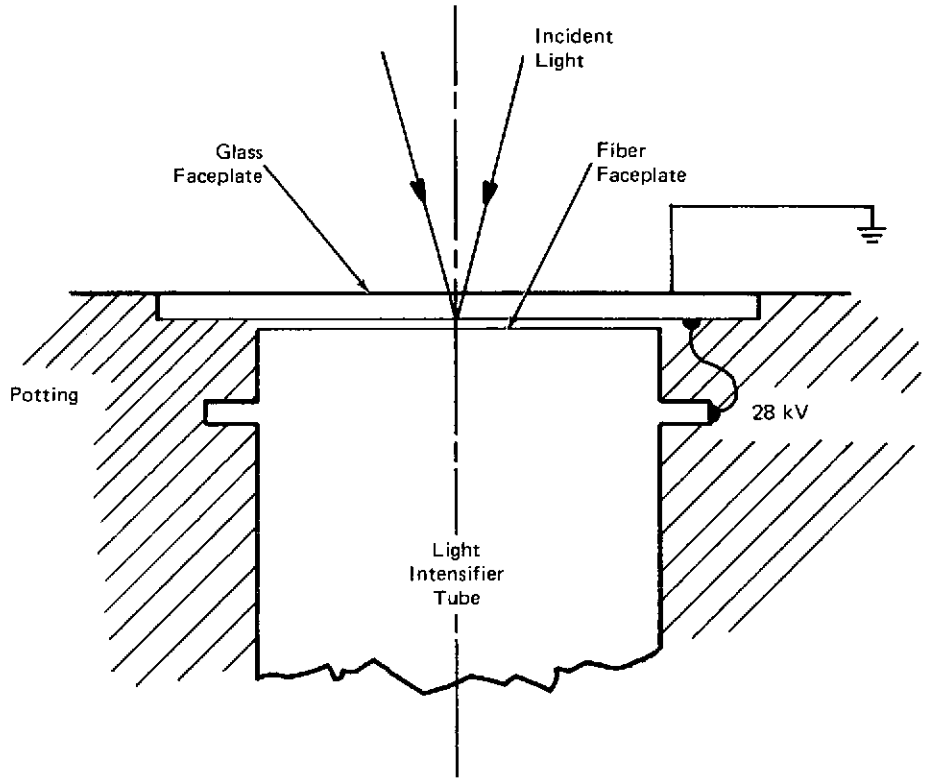
$$I_{load} \approx \frac{V_{BE}\,(Q2)}{R1}$$

In addition to current limiting capabilities, this circuit has potential application as a solid state relay when peak current limiting is required. This can be accomplished by returning R2 to ground through a low-level switching device such as a transistor or relay.

Source: W. R. Lombs of
RCA Corp.
under contract to
Goddard Space Flight Center
(GSC-10070)

Circle 1 on Reader Service Card.

CAMERA CORONA SHIELD



A method has been developed to remove voltage gradients from fiber faceplates of TV cameras utilizing light intensifier tubes. A glass plate coated with a transparent electrically conductive coating is mounted in front of the intensifier tube and connected to ground (see fig.). In the presence of a partial vacuum, dirt, or humidity, the use of the plate prevents corona discharge and the possible failure of the fiber faceplate. The entire assembly is potted with a silastic rubber to provide a high resistance to surface leakage. An additional benefit of this method is improved suppression of external source EMI due to the low resistance ground plane.

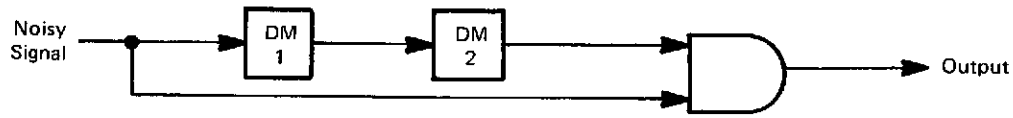
The vacuum deposited coating of optical quality produces an average loss of only 2.5 percent within the spectrum of interest. Electrostatic voltage gradients still exist on the faceplate, distributed from the photocathode through the fiber faceplate, the air gap, and the glassplate, and radially to ground. The radial paths, however, are generally longer than the longitudinal path.

This technique should be useful in extending the operating life of image intensifier television cameras. It should be of particular benefit for cameras used in remote surveillance and industrial security applications.

Source: F. J. Kaisler and H. I. Bull, Jr., of
Westinghouse Electric Corp.
under contract to
Johnson Space Center
(MSC-13856)

Circle 2 on Reader Service Card.

ANTI-NOISE CIRCUIT



A circuit for eliminating the effects of contact bounce (from mechanically actuated components) in high speed electronic circuitry has been developed. The desired output is obtained in synchronization with the contact closure.

The anti-noise circuit (see fig.) consists of two delay multivibrators and a gate. The first delay multivibrator is triggered by a negative-going pulse generated by the contacts either opening or closing. After a time determined by the contact settling time, the delay multivibrator triggers a second delay multivibrator. The output of this second delay multivibrator is applied to an AND gate with the second input connected to the noisy signal source. The resulting output pulse is a combination of the second delay multivibrator being triggered and the presence of the signal.

This technique could be useful as another method for solving the electromechanical device/electronic circuit contact bounce interface problem.

Source: J. S. Ferguson of
Rockwell International Corp.
under contract to
Johnson Space Center
(MSC-15786)

No further documentation is available.

MODIFICATION OF STANDARD NTSC COLOR MONITORS FOR OPERATION WITH SEQUENTIAL COLOR SIGNALS

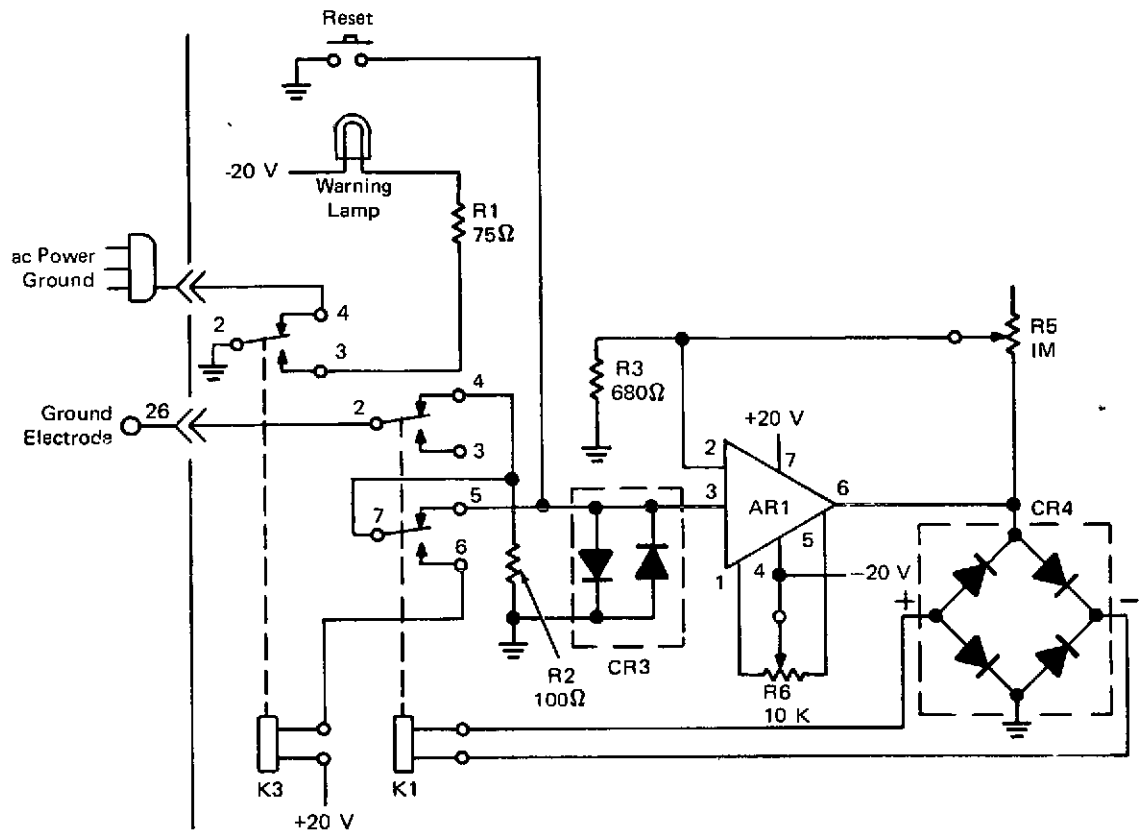
Standard commercial and industrial color monitors derive the required CRT signals by demodulating the color subcarrier contained in the National Television System Committee (NTSC) signal. For sequential color input signals, the monitor does not receive any subcarrier; it reverts to monochrome operation. The proposed modification permits normal operation except only one color is allowed to be presented during each field of the incoming signal by adding pulses into the video amplifiers of the monitor. These pulses are derived from the monitor sweep circuits and are controlled by a divide-by-three ring counter to provide the proper color sequential display. The monitor amplifiers sense these pulses and effectively blank two of the three CRT electron guns by driving the video on these guns below the black level during any field. The ring counter moves one count during each vertical blanking interval, allowing a different color to be displayed in synchronization with the incoming sequential signal. To provide phasing between the video and the counter, a rotary switch is provided on the front panel of the monitor, replacing the degaussing pushbutton. The degaussing function is included as one position on this switch, as is normal when the monitor operates without sequencing.

The circuitry is installed on an electronic circuit plug-in board added to the monitor; and connections are made between this board, the vertical deflection and blanking board, and the matrix board. Power for operation of the circuit is tapped from the matrix board.

Source: Westinghouse Electric Corporation
under contract to
Johnson Space Center
(MSC-13650)

Circle 3 on Reader Service Card.

GROUND PROTECTION DEVICE FOR BIOINSTRUMENTATION



Ground Electrode Protection Circuit

A ground protection device is incorporated into a biomedical recording system to protect the subject from electrical shock hazard while the EKG electrodes are attached to his body and the system is plugged into a 115 V, 60 Hz receptacle. This protection is provided for all operational and failure modes of the system.

Bioinstrumentation commonly used in clinics provides no positive measure of electrical shock protection. Standard practice is to either completely isolate the chassis of the equipment from power ground or alternatively the ground side of power sources in the equipment is connected to the chassis; the chassis then is connected to the power line ground through the ground wire of the power plug or a separate ground wire through the third prong of a three prong plug. In both of these approaches, equipment failure or building wiring failures can create a dangerous electrical potential between the subject connected to the equipment and true ground.

The ground protection device used in the recording system senses current flow through the ground electrode attached to the subject, and when the current exceeds approximately 100 microamperes, power circuits are disconnected within less than two milliseconds.

Optimum signal data quality is obtained when the subject is electrically connected to signal ground. This connection however produces a dangerous shock hazard unless there are provisions to limit maximum current flow through the subject's body. The ground protection circuit design provides for automatically disconnecting the subject from ground when the ground circuit current exceeds the predetermined level. The figure shows a schematic diagram of the circuit which operates in the following manner:

(1) Any potential greater than approximately 15 mV entering the ground protection circuit on pin 26 into K1 (2-4) causes circuit activation. A positive or negative voltage is developed on pin

3 of AR1 across R2 and CR3. Input sensitivity is adjustable by R5 in the feedback circuit. Complete saturation of AR1 is needed to affect the latching of K1 and K3 through CR4; this is accomplished by the opening of K1 contacts 7 and 5.

(2) R6 of AR1 is the internal dc offset control. It is used to set the output of AR1 to 0 Vdc with the reset switch closed. CR3 is used to protect the input to AR1.

(3) Resistance R2 is used in series with the input to develop a voltage drop. It also serves to limit current to K3 during the protection mode.

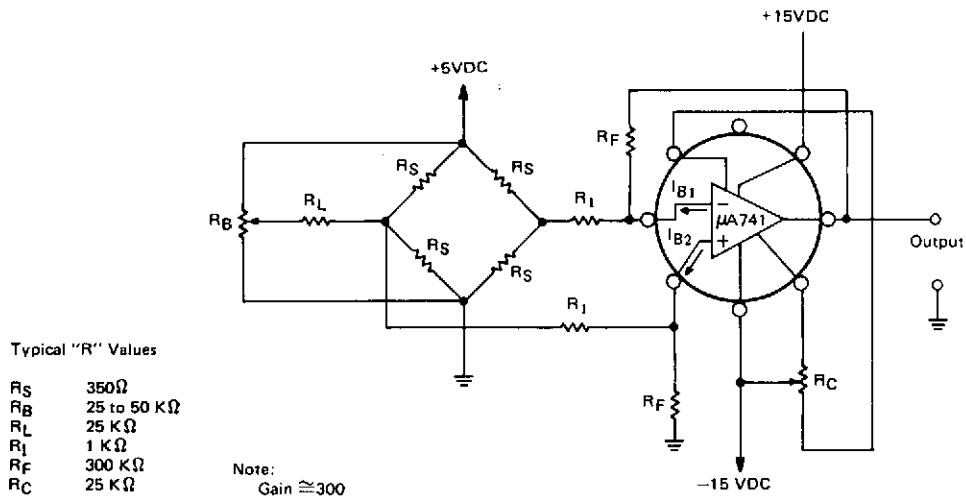
(4) After approximately 1 ms, the contacts on K1 (2-4) open, breaking the patient ground (pin 26). At the same time, K3 is energized through K1 (6-7) and R2 to the power supply ground. Contacts on K3 (2-4) also open breaking continuity between power supply ground and ac power ground. The other contact on K3 is used to supply a ground return from -20 Vdc to light the warning indicator lamp.

(5) When the reset button is pressed, the grounded input of AR1 causes the output to return to 0 Vdc, and K1 de-energizes causing K3 to do the same. The patient is then grounded, and the warning indicator lamp goes out.

Source: H. A. Vick of
Northrop Corporation, Electronics Div.
under contract to
Johnson Space Center
(MSC-13654)

No further documentation is available.

TEMPERATURE COMPENSATION FOR OPERATIONAL AMPLIFIERS



Many integrated circuit operational amplifiers provide taps for external balance circuits to facilitate output offset adjustment. In the typical application (see figure), offset is provided by the R_B and R_1 network which is normally associated with a bridge type transducer (R_S). In this application, the amplifier offset taps are available for temperature compensation.

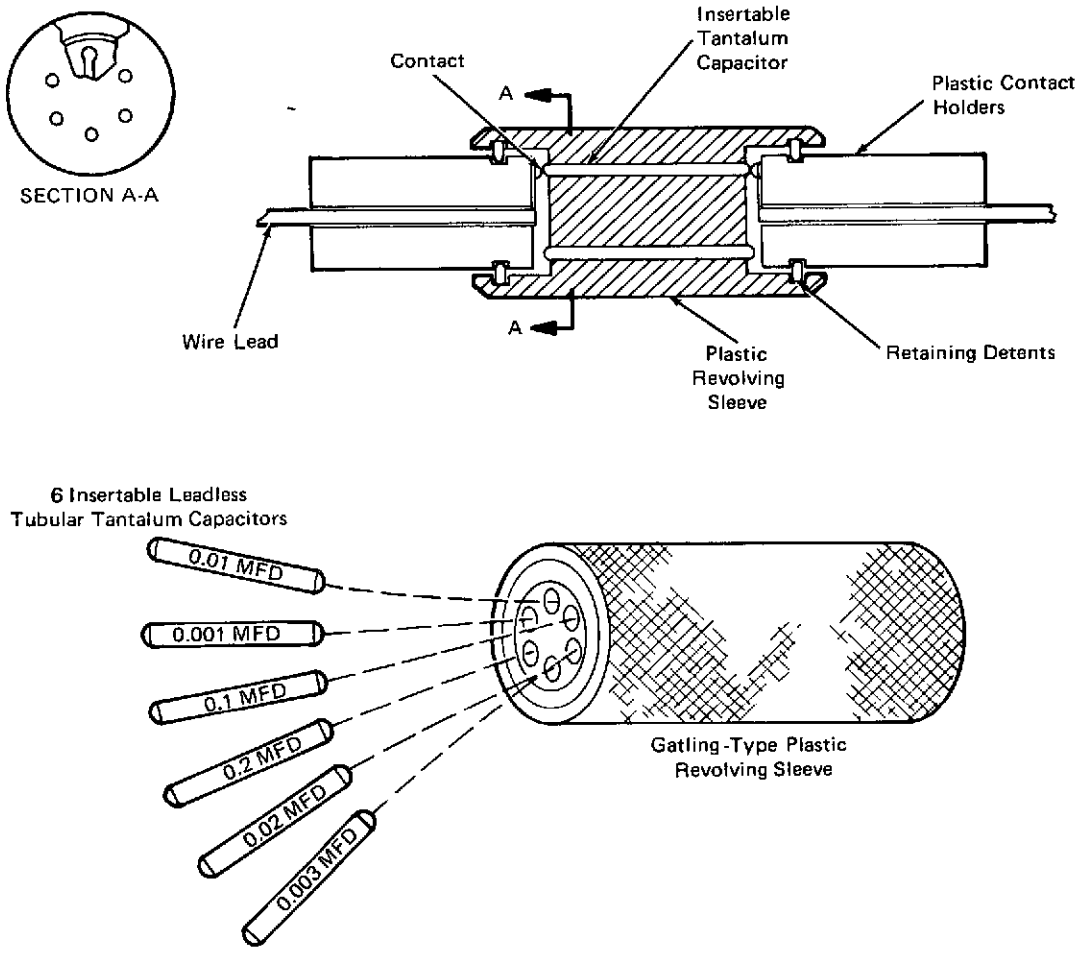
A carbon composition trimmer (R_C) provides adjustment of temperature coefficient to compensate for the effects of mismatched input bias currents. Repetitive adjustments are made, and subsequent circuit performance is observed to accomplish optimum stabilization.

Note that final output offset adjustment should be made by adjusting R_B after completion of temperature compensation operation.

Source: K. M. Murphy and R. R. Walker of
Rockwell International Corp.
under contract to
Johnson Space Center
(MSC-17905)

No further documentation is available.

HYBRID GATLING CAPACITOR



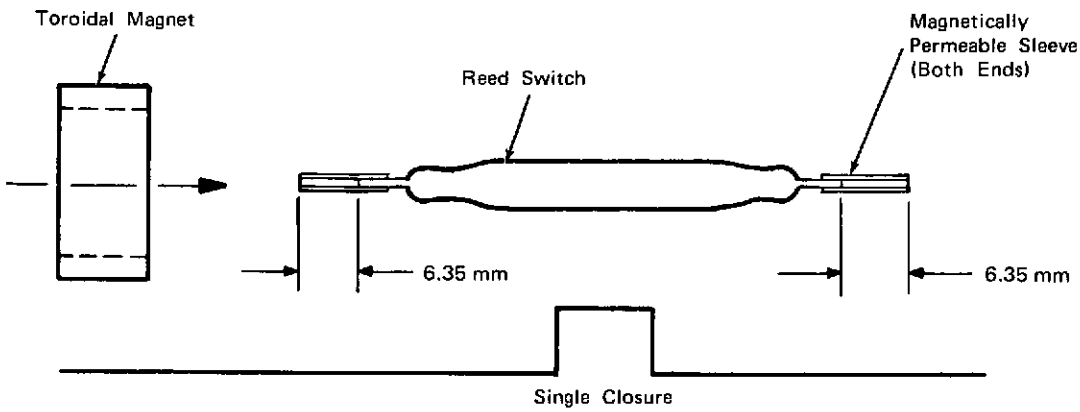
Due to circuit deterioration, component tolerance changes, and changes caused by extreme environmental conditions, adjustments have to be made in the capacitance of RC networks of certain electrical/electronic circuits. The present methods of changing capacitance include a patch cord plug-in unit that allows switching from one capacitor in the patch cord unit to another.

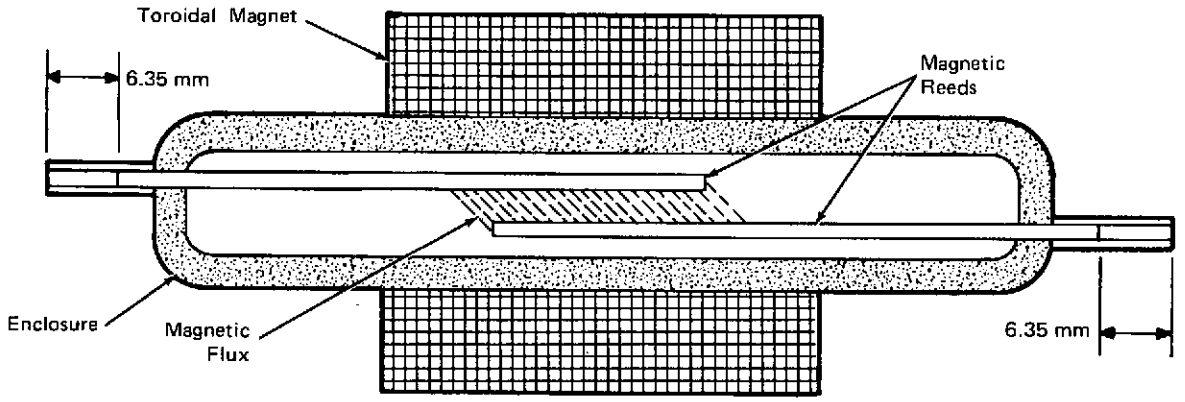
Using the Gatling-type principle whereby the proper capacitance value can be brought into the circuit easily, the optimum circuit capacitance can be obtained. A revolver cylinder-type sleeve, having six easily insertable tantulum capacitors with button type contacts instead of leads (see fig.), is installed in the circuit. Capacitance change is accomplished by merely turning the knurled holder until the proper capacitance value is obtained. Replacement of any of the six capacitors with one of a different value is done by disconnecting the rhodium contact holders and removing the capacitors like batteries being removed from a flashlight. Rhodium is used for contacts to eliminate detrimental effects of arcing during the process of changing from one capacitance value to another using the Gatling principle.

Source: R. Manoli and B. R. Ulrich of
Rockwell International Corp.
under contract to
Marshall Space Flight Center
(MFS-16723)

Circle 4 on Reader Service Card.

PREVENTION OF MULTIPLE CLOSURES OF REED SWITCHES





A system to accurately measure the level of a liquid in a tank utilized a series of reed switches installed at discrete levels in a tube mounted vertically in the tank. A toroidal magnet surrounding the tube was mounted on a float. As the liquid level dropped, the magnet on the float would activate the reed switches. However, as the magnet passed completely over a reed switch, it would cause three closures; once on each end, and once in the middle. To prevent this, the magnets have been weakened by partial degaussing. This, however, makes the center closures less reliable.

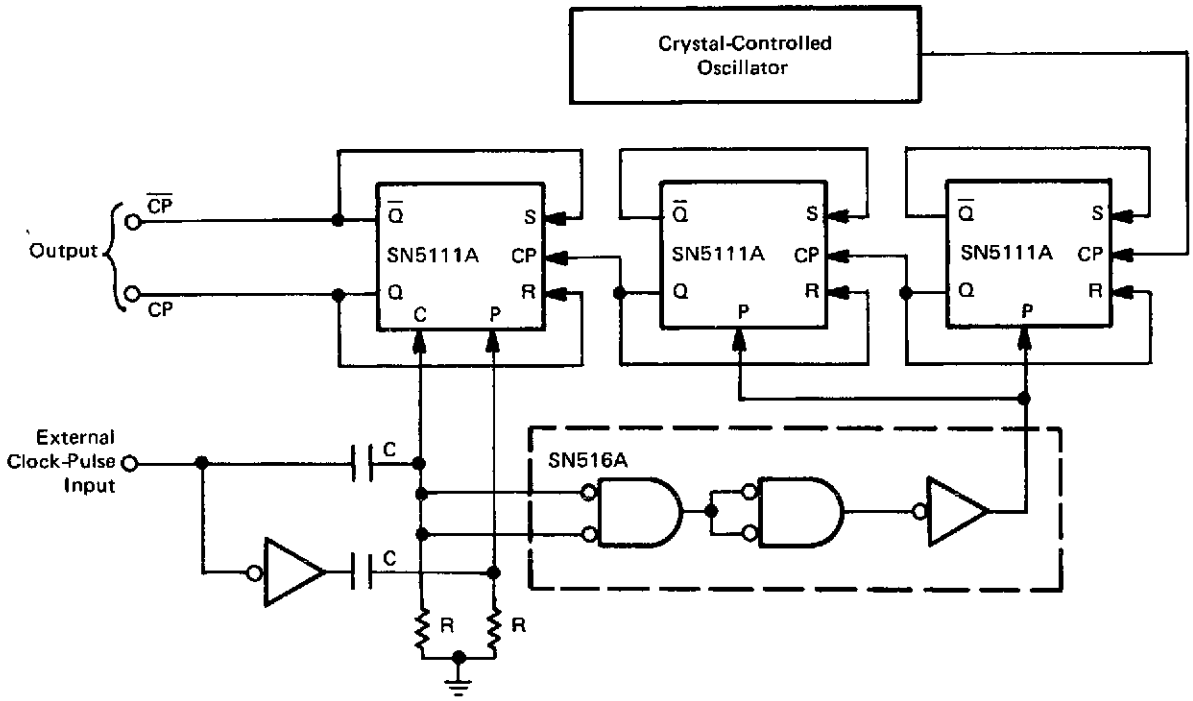
By adding magnetically permeable sleeves (see fig.) which extend the ends of the switch reeds by 6.35 mm, the magnet is prevented from establishing a field that will close the reeds when it passes over the reed ends.

The magnetic path at each end of the switch is lengthened by attaching a piece of magnetically permeable material concentric with the switch centerline. This prevents establishment of the magnetic path which causes the outer closure. Lengthening the path only 6.35 mm prevents multiple closures when used with a full strength toroidal magnet of the type normally employed in the liquid level gage. Reliability of the center closure is enhanced by the greater strength of the magnet. This method is simple, inexpensive and compact. It may even be designed as a sleeve which will serve a second purpose, that of facilitating wire attachment.

Source: L. H. Groeper of
North American Aviation, Inc.
under contract to
Marshall Space Flight Center
(MFS-90849)

No further documentation is available.

MICROMINIATURE CRYSTAL-CONTROLLED CLOCK SYSTEM CAPABLE OF EXTERNAL SYNCHRONIZATION



The circuit shown in the figure was designed to fill a need for a microminiature clock system capable of operating in either of two modes: (1) controlled by a precision internal oscillator, or (2) in exact synchronization with an external clock. The solution was the use of a crystal-controlled oscillator operating at 2^n times the desired repetition rate, followed by n bistable multivibrators with external clock pulse synchronization applied to the last multivibrator in the series circuit.

A crystal-controlled oscillator normally operates at a much higher repetition rate (frequency) than the clock rate of most multiplexers to minimize crystal size and to improve vibration and reliability characteristics. Therefore, countdown multivibrators would normally be used to derive the desired clock frequency from an oscillator signal as shown in the figure. By using multivibrators with dc set and reset capability (such as the Preset and Clear inputs on the SN5111A), external synchronization may be attained by adding only two capacitors, two resistors, and three NAND gates (contained in a single SN516A circuit element).

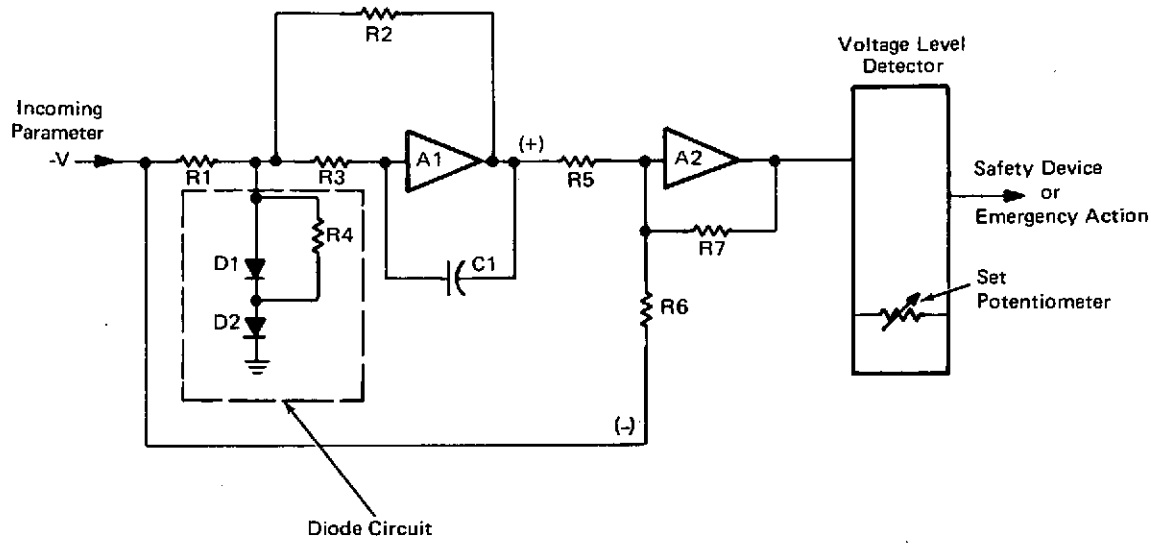
The leading and trailing edges of the input signal are differentiated by RC circuitry. The resulting spikes are used to control the output multivibrator directly, so that both the repetition rate and the duty cycle are precisely reproduced. The spikes are also summed and used to preset the higher-frequency multibivrators, preventing internal oscillator signals from passing through the multivibrators. To accomplish this oscillator signal blocking, the time constant of the RC differentiating circuits must be greater than the period of the oscillator signal applied to the first multivibrator in the series.

Since the synchronization input is capacitively coupled, its dc level is not important. If external synchronization is lost, the multivibrator presetting signals will also be lost, and signals from the internal oscillator will pass through the multivibrators to provide a clock-pulse output for the system.

Source: W. A. Maasberg of
IBM Corp.
under contract to
Marshall Space Flight Center
(MFS-13229)

No further documentation is available.

CIRCUIT DETECTS PARAMETER FAILURE



A circuit has been designed to obtain a voltage signal that will initiate timely action in case the rate-of-change of a selected, measured parameter (temperature, pressure, flow, etc.) exceeds a predetermined limit.

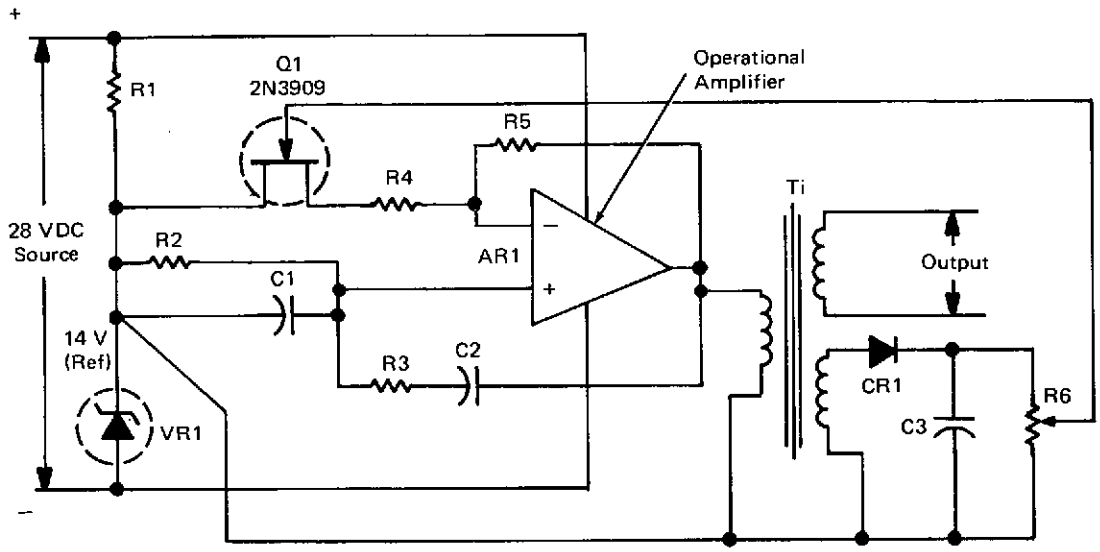
A diode network is inserted in a tracking and comparison circuit network (see figure). The diode network is selected to provide tracking of an incoming parameter at the output of amplifier A1, up to the normal rate-of-change of the parameter selected.

The parameter to be monitored for excessive rate-of-change is connected as shown to operational amplifiers A1 and A2. Amplifier A1 provides integration and lag action, and has a diode network (D1, D2, and R4) which conducts to limit the rate at which the amplifier output can change. When the input parameter changes rapidly, the voltage signal into amplifier A2 from A1 will lag the direct signal. Amplifier A2 will compare the two voltage signals and generate another output signal. Since amplifier A1 cannot follow a rapid rate-of-change, this output signal will be used to trip the voltage level detector initiating a safety device or other required emergency action. The amount of deviation of the output signal to cause the trip action may be set by the set potentiometer on the level detector. For the amount of error to be a function of the operating voltage level, resistors R5 and R6 are unbalanced. The ratio of resistance of R7 to R5 and R6 determines the gain of amplifier A2. In the specific case where this circuit was applied the failure event was detected and emergency action was initiated prior to completion of the actual failure event.

Source: F. L. Openshaw of
Aerojet-General Corp.
under contract to
AEC/NASA Space Nuclear Systems Office
(NUC-90055)

Circle 5 on Reader Service Card.

ISOLATED FEEDBACK FOR LOAD REGULATION



This circuit (see figure) illustrates the use of an additional secondary winding on a transformer to provide an isolated feedback circuit for load regulation. The feedback source is connected after the output stage, yet it provides for isolation between load and feedback circuit. Usually, feedback circuits are connected to the load or connected ahead of the output stage.

The circuit operation provides the following features:

(1) The desired output is set by potentiometer.

(2) Voltage changes due to loading of the output winding are reflected as R6 is moved, and this will offset FET Q1 to return the output voltage to the preset value (gate polarity is not important).

(3) Actual component values will vary with application.

Source: J. B. Lindsay and L. S. Wright of
Rockwell International Corp.
under contract to
Johnson Space Center
(MSC-11462)

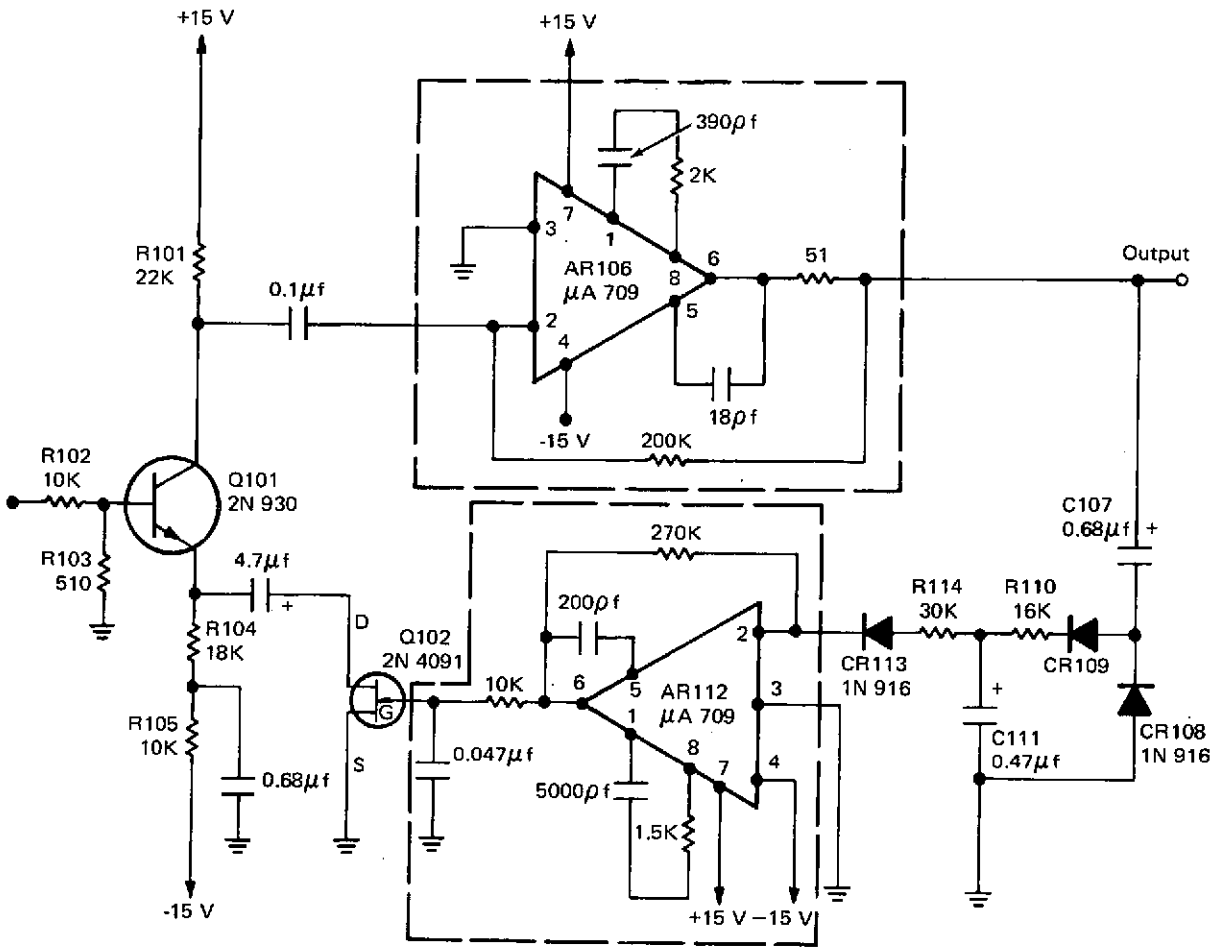
No further documentation is available.

AUTOMATIC SIGNAL RANGE CONTROL

The electronic circuit shown in the figure provides a means of reducing the signal dynamic range in a television system while maintaining the modulation detail.

The modulated signal contains the slowly varying dc component representing the average scene illumination and the rapidly changing or high frequency component representing the change in brightness within the scene. The automatic signal range control circuit is used to suppress the slowly changing video component and to retain the detail high frequency information of the scene. The circuit compresses the dynamic range of the signal so that it may be within the acceptance levels of a tape recorder. By this means, signal loss due to recorder-noise masking at low level recording, and signal distortion due to tape saturation at high level are eliminated. The innovation consists of a variable gain amplifier, a straight-through amplifier for high frequency components and a low frequency amplifier in a feedback circuit driving the variable gain amplifier to control the gain at low frequencies.

Refer to the figure, specifically to transistor Q101 with its input voltage divider network consisting of resistors R102 and R103, load resistor R101, feedback resistor R104, and isolation resistor R105 in the emitter circuit. Transistor Q101 is used as the variable gain amplifier stage. A change in the effective emitter



circuit resistance occurs when the field effect transistor (FET) Q102 changes its resistance to ground. When the FET is open, the emitter of transistor Q101 sees only the 18K resistance R104, and the stage gain is minimum. When the FET is closed, i.e., the source to drain resistance of the FET reduces to about 30 to 40 ohms under control of a signal at the gate, the 30 to 40 ohms resistance is in shunt with the 18K resistance of R104, providing maximum gain for the Q101 amplifier stage.

High frequency signals are coupled directly through the straight-through integrated circuit amplifier stage AR106 to the output terminal. However, the low-frequency discriminating feedback loop consisting of integrated circuit amplifier AR112 and associated circuitry drives the FET to vary the gain of the input stage. Thus the automatic signal range control circuit acts as a high-pass filter to reduce the amplitude of the low frequency components of a video signal without affecting the high frequency components.

Diodes CR108 and CR109, resistors R114 and R110, and capacitor C111 form a voltage-shaping network for the input signal to feedback amplifier AR112.

Source: R. Y. Wong of
Cal Tech/JPL
under contract to
NASA Pasadena Office
(NPO-10702)

Circle 6 on Reader Service Card.

A DIGITAL AUTOMATIC GAIN CONTROL CIRCUIT

The gain control element is an electronically switched resistive attenuator, shown in Figure 1. The attenuator is an "L" voltage divider with a transistor switch Q_1, in series with the shunt branch of the network. When transistor Q_1 is saturated, the voltage output will be:

$$V_{output} = \frac{R_2 + R_{Q_1}}{R_1 + R_2 + R_{Q1}} \text{(input signal voltage)}$$

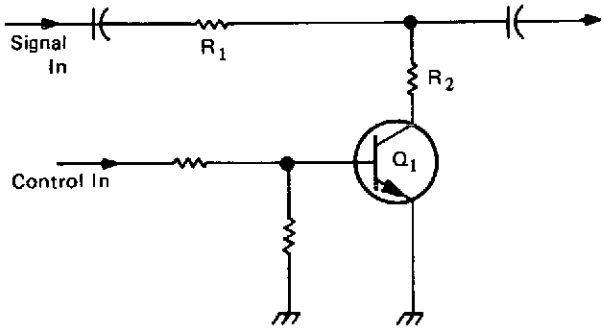


Figure 1

The gain control system operates as follows: When the detected output of the IF amplifier exceeds the reference level, the comparator turns on a clock. The clock drives a counter, which turns on the attenuators in sequence as long as it is receiving clock pulses. This process continues until the detected output of the IF amplifier falls below the reference. When this occurs, the clock stops and the counter holds.

The digital AGC has several advantages over commonly used analog AGC circuits, particularly in the areas of calibration and gain resetting. Because the gain is adjustable in a fixed number of discrete steps, it is practical to calibrate the receiver for all possible gain settings. In contrast, an analog AGC circuit theoretically produces an infinite number of gains, making it impractical to calibrate at all gain settings. Further, the actual gain setting of the digital AGC is easily determined by noting the state of the switches that drive the attenuators. Analog AGC systems usually require the measurement of a continuous-range voltage in order to determine the gain of the receiver. This method is impractical for use in the radar scattering-coefficient measuring instrument because of the possible introduction of errors.

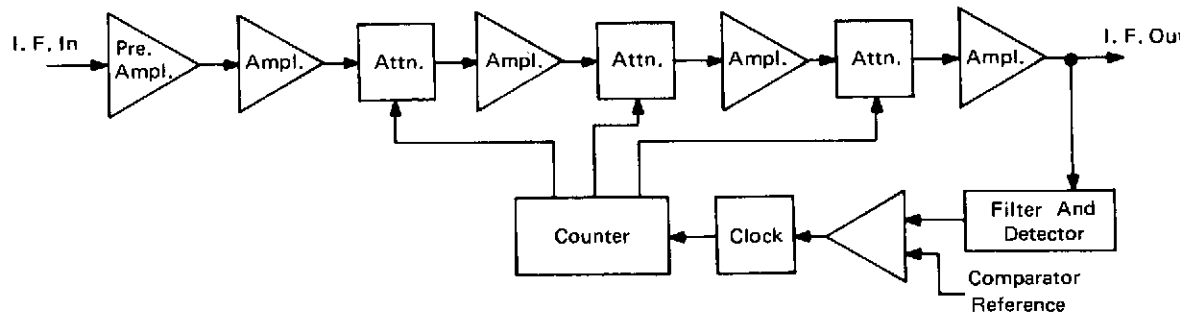


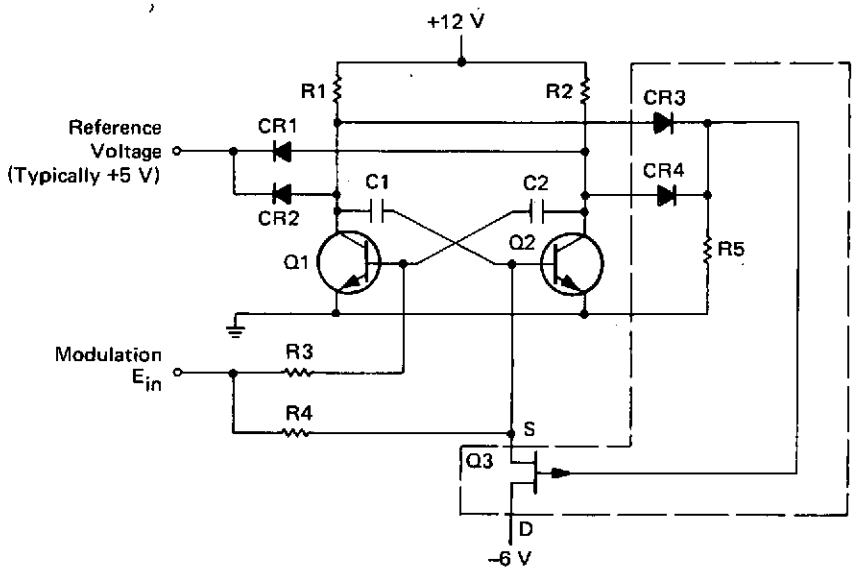
Figure 2

The resistance R_{Q_1} represents the equivalent resistance of the transistor Q_1 when it is saturated. Since R_{Q_1} is small compared with R_1 plus R_2, the effects of R_{Q_1} can be neglected. The gain control system is made up of a cascade of gain stable amplifiers and electronically switched attenuators combined with logic circuitry to drive the attenuators as shown in Figure 2.

Source: L. W. Counts of
Massachusetts Institute of Technology
under contract to
NASA Headquarters
(HQN-10238)

No further documentation is available.

ANTI-STALL CIRCUIT



A recent program involved the development of a compact FM record and reproduce amplifier for recording and reproducing FM data on magnetic tape.

Generally, the carrier in an FM record amplifier is generated by an astable multivibrator whose frequency is caused to deviate in a linear fashion by the impressed data. Many versions of such circuits have been used, the most common being a simple cross-coupled pair of transistors. However, such a circuit has the disadvantage that when power is initially applied, both transistors may turn on in a saturated condition and the circuit will not oscillate.

Again, there are various means of protecting against such failure. However, most such circuits used in the past have undesirable side effects such as introducing additional temperature drift of the oscillator.

This innovation provides an assurance circuit for a frequency deviated multivibrator (voltage controlled oscillator) which guarantees that the oscillator will not stall. Even if the circuit attempts to stall after initial operation (due to some perturbation in the system), this circuit will cause oscillation to recommence and does not rely on reapplication of supply power.

The figure is a schematic of the circuit with the components making up the anti-stall section enclosed in dotted lines. The remainder of the circuit is a typical voltage controlled oscillator. Operation is as follows:

When the multivibrator is operating normally (i.e., Q1 and Q2 are alternately switching on and off), a positive dc voltage of approximately 5 V is developed across resistor R5 due to diodes CR3 and CR4. This voltage is applied to the gate of Q3, thus cutting off Q3, which then has no effect on the multivibrator operation. However, if both Q1 and Q2 should remain on in a stalled condition, the positive gate voltage for Q3 disappears since the anodes of CR3 and CR4 are both held near ground. At this time, Q3 will start to conduct and take base current from Q2, thus forcing Q2 to come out of saturation. As Q2 comes out of saturation, its collector voltage rises, re-establishing oscillation and again generating the cut-off bias for Q3.

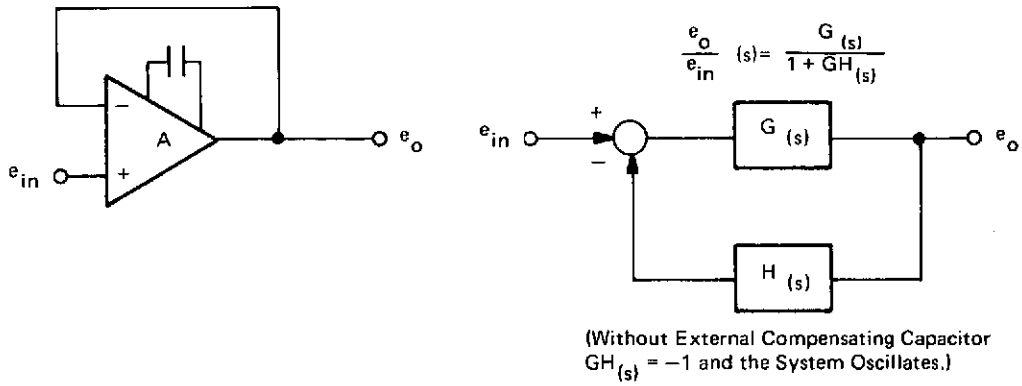
The unique features of this anti-stall circuit are:

(1) It has virtually no effect on the oscillator circuit during normal operation.
(2) It consumes essentially no power during normal operation.
(3) It guarantees restarting in case of stall without the need to reapply input power.

Source: A. E. Fisher of
Almond Instrument Company
under contract to
Johnson Space Center
(MSC-13807)

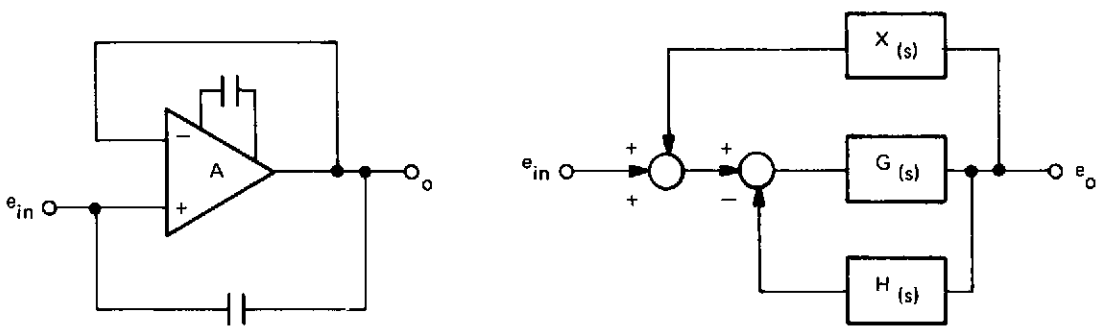
No further documentation is available.

POSITIVE FEEDBACK STABILIZATION OF OPERATIONAL AMPLIFIERS



(Without External Compensating Capacitor $GH_{(s)} = -1$ and the System Oscillates.)

Figure 1. Conventional Operation



$$\frac{e_o}{e_{in}}(s) = \frac{G_{(s)}}{1 + G_{(s)}\,[H_{(s)} - X_{(s)}]}$$

(By Proper Choice of $X_{(s)}$ The System Can Be Stabilized And Better Performance Can be Achieved Than By The Conventional Use Of An External Compensating Capacitor To Alter The Characteristics Of $G_{(s)}$.)

Figure 2. Positive Feedback Stabilized Operational Amplifier

Instability in integrated circuit operational amplifiers very often occurs when they are operated in a closed loop configuration. The problem becomes acute when the amplifier is operated as a unity gain voltage follower. In this instance, the highest degree of negative feedback is applied and requires the largest amount of compensation to maintain the desired stability. The compensation usually takes the form of a capacitor placed externally between the outputs of a differential stage someplace in the amplifier (see Figure 1). The introduction of this capacitor lowers the slew rate greatly because of the inherent time constant associated with the charge and discharge of the compensating capacitor.

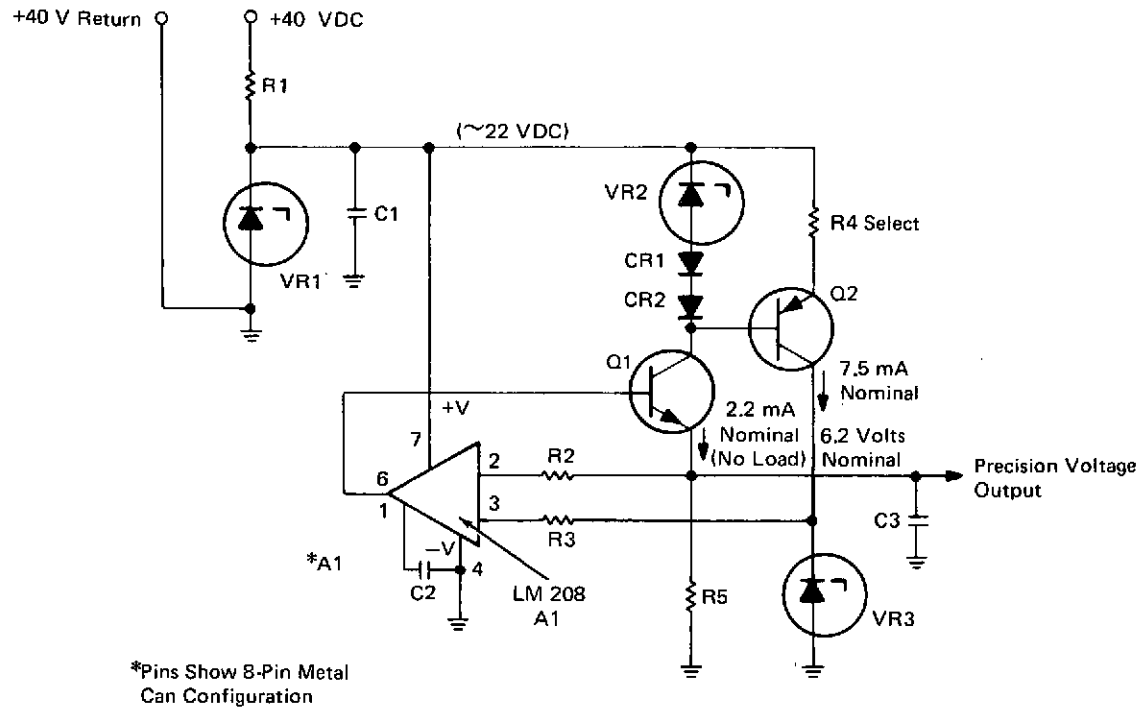
Instead of following convention, the amplifier may be stabilized by using positive feedback. (Positive feedback has usually been thought of as undesirable since it tends to destabilize a system. However, under certain circumstances, it can be beneficial and gives an added dimension of freedom to the circuit designer.)

The use of positive feedback will allow either the elimination of the compensating capacitor or the use of one with a small capacitance value. In any case, the slew rate performance of the amplifier is greatly improved when compared to the conventional scheme (see Figure 2).

Source: A. J. MacMillan of
TRW, Inc.
under contract to
Marshall Space Flight Center
(MFS-21443)

Circle 7 on Reader Service Card.

VOLTAGE REGULATION CIRCUIT



Voltage Regulation Circuit

A novel regulation circuit contributes to the design of an active voltage stabilization system. The circuit (see figure) consists of a decoupling network with a Zener diode connected to a feedback controlled operational amplifier.

The main portion of the electronics is decoupled from the input power by resistor R1, Zener diode VR1, and capacitor C1. The voltage derived from the decoupling network is –22 volts dc which is regulated by VR1 and used to power the rest of the electronics. The network consisting of VR2, CR1, CR2, R4, and Q2 forms a current source, supplying current to the precision Zener reference VR3. Diodes CR1 and CR2 provide temperature compensation for the current source. The amplifier A1 is a low input bias current (3.0 nanoamps maximum) amplifier also having high open loop gain (80,000 volts/volt minimum) and low voltage offset change with temperature (5 μV/K maximum). The amplifier is used in a closed loop configuration so as to maintain the output voltage equal to the precision Zener voltage plus or minus the input offset of the amplifier. In closing the feedback loop, current is set through VR2 by establishing the precision voltage across R5. As Q1 and Q2 are high current gain transistors, the current passing through R5 is essentially the current that passes through VR2.

The advantages of this circuitry may be summarized as follows:

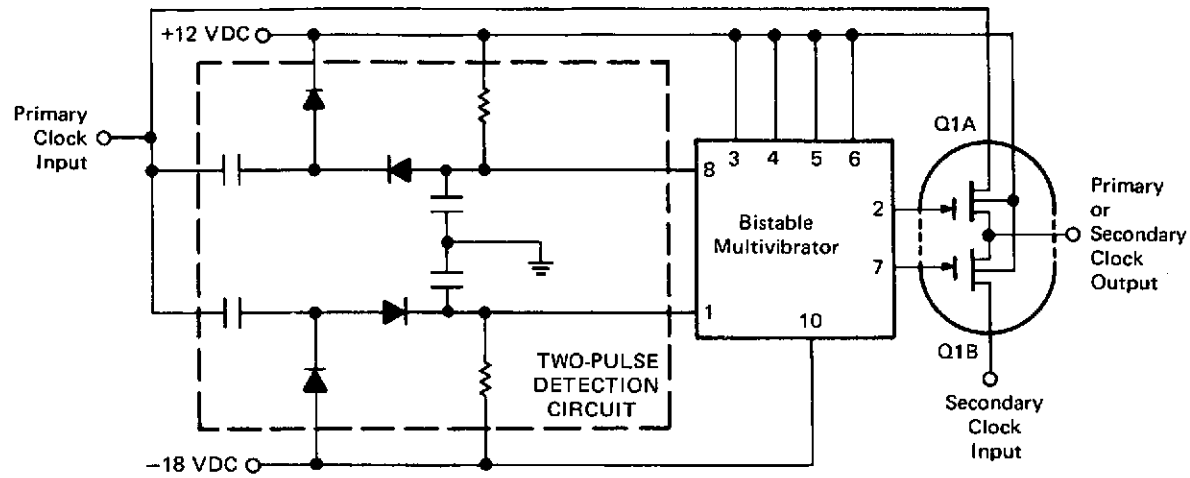
(1) The current through the precision Zener is controlled.
(2) The output impedance is very low ($<0.001\ \Omega$).
(3) A flat voltage output versus temperature characteristic may be attained by changing the value of R4 and therefore changing the current through, and the temperature coefficient of, VR3.

This innovation may therefore be useful as a power supply regulator for test instruments such as multimeters, solid-state oscilloscopes, etc.

Source: L. W. Newberry, Jr., of
Honeywell, Inc.
under contract to
Johnson Space Center
(MSC-13795)

No further documentation is available.

INTEGRATED CLOCK-SWITCHING CIRCUIT



The circuit shown in the figure is designed to switch from a primary clock input to a secondary clock input if the primary clock input is not received for four or more counts.

With a primary clock input received, the two-pulse detecting circuit sets the bistable multivibrator. A set signal from pin 2 of the multivibrator will enable metal oxide semiconductor (MOS) Q1A, thus enabling the primary clock output. If the primary clock is removed, the bistable multivibrator (any conventional integrated circuit multivibrator) is reset by the two-pulse detecting circuit. A reset signal from pin 7 of the multivibrator will turn on MOS Q1B, thus connecting the clock output to the secondary clock input through Q1B.

The circuit tested is operational from 50 Hz (primary clock) through 100 kHz.

Source: G. N. Miller and H. F. Smith of
IBM Corp.
under contract to
Marshall Space Flight Center
(MFS-14811)

No further documentation is available.

INEXPENSIVE PASSIVE THERMAL PROTECTION FOR SOLID STATE POWER SUPPLIES

A coil of variable resistance wire wrapped around an element of a transistor heat sink provides an inexpensive method of protecting a solid state power supply from thermal damage caused by short circuits or overloads.

The coil, illustrated in Figure 1, is Number 40 pure nickel wire which has a high temperature coefficient. It is wound around a portion of the output transistor heat sink in the final power supply stage. A piece of shrinkable tubing, slipped over the heat sink element and the wire, holds the coil in place and helps to limit heat dissipation.

The wire has a nominal resistance of one ohm at 298.15 K, and it increases substantially in resistance as its temperature rises. The heat sensitive coil acts as a control element (R_{CS}) in a thermal feedback loop of the output transistor. Refer to Figure 2 for circuit location. When an overload or short circuit causes a temperature rise, the resistance of the nickel wire increases, reducing power supply output current. For the power supply illustrated, a 100 K rise in heat sink temperature resulted in a 40 percent decrease in output current.

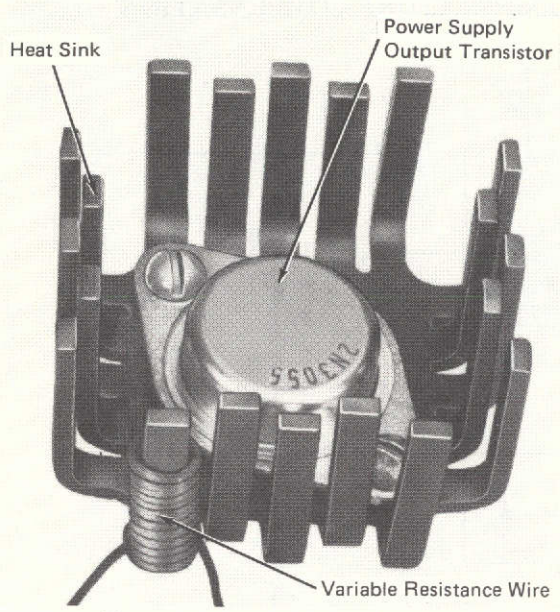


Figure 1. Heat Sink and Sensing Coil

The heat sink and the coil must be electrically insulated from each other, and the leads of the coil must be plated for soldering.

This method of thermal protection provides an inexpensive alternative to active sensing elements, such as temperature sensing diodes and transistors in solid state dc power supply design. It does not interfere with the current regulation of the power supply under normal load conditions.

Source: K. M. Murphy and R. R. Walker of
Rockwell International Corp.
under contract to
Johnson Space Center
(MSC-17418)

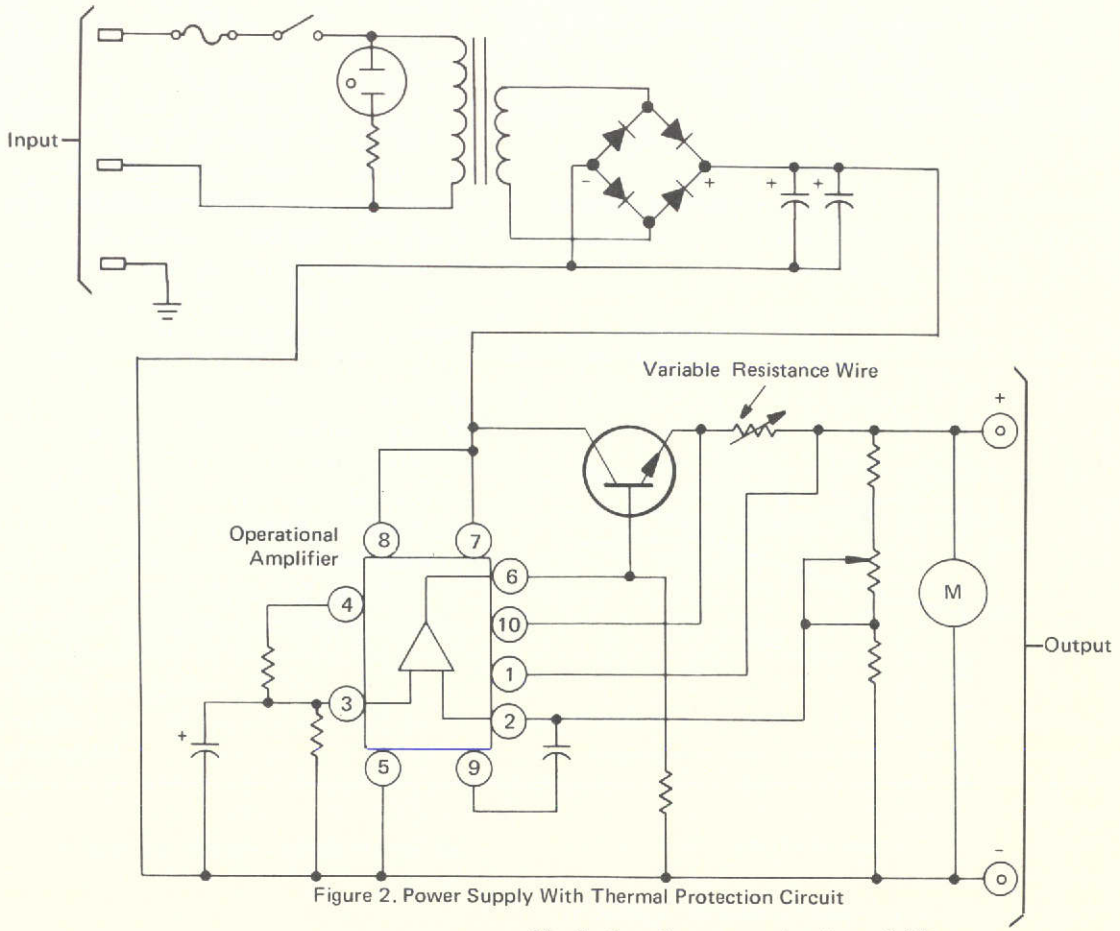


Figure 2. Power Supply With Thermal Protection Circuit

No further documentation is available.

POWER SUPPLY REGULATOR TEMPERATURE COMPENSATION

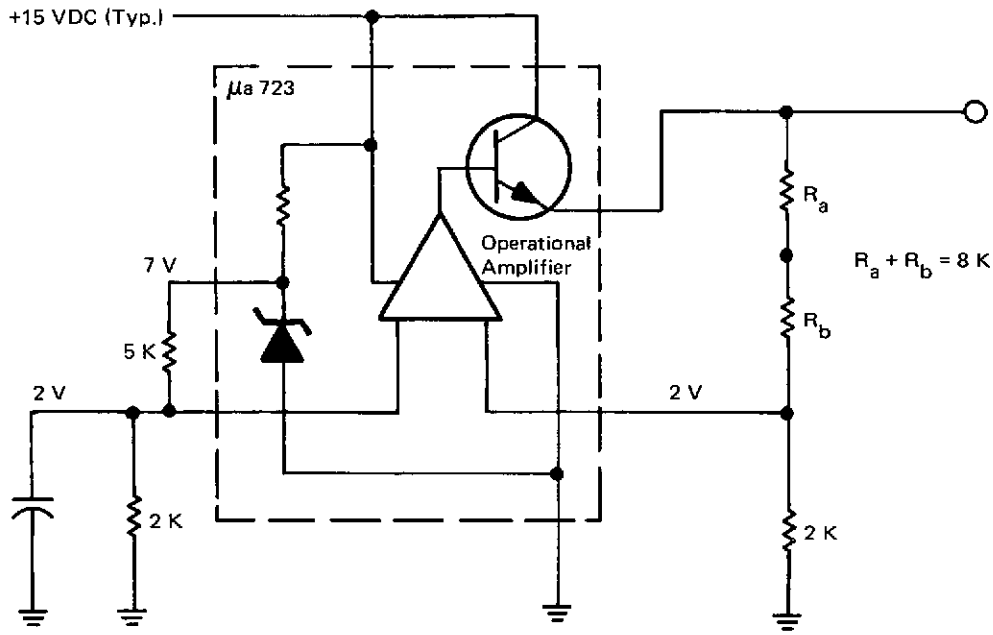


Figure 1. Schematic

Many of the integrated circuit regulators in popular use today have undesirable coefficients of output voltage with respect to temperature. This innovation provides a convenient means for minimizing this coefficient at negligible cost.

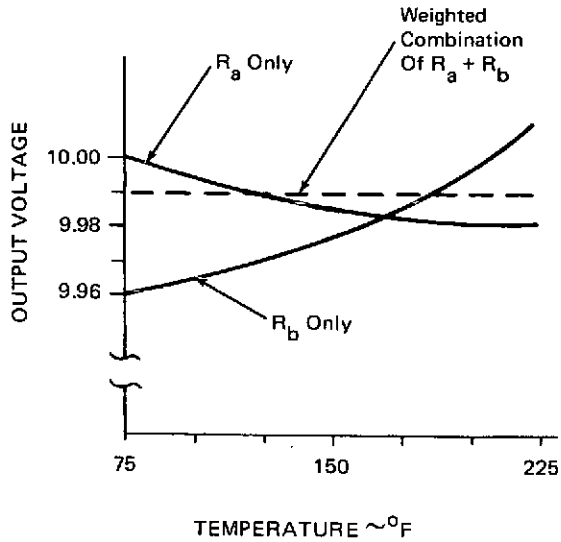


Figure 2. Typical Output Temperature Coefficients

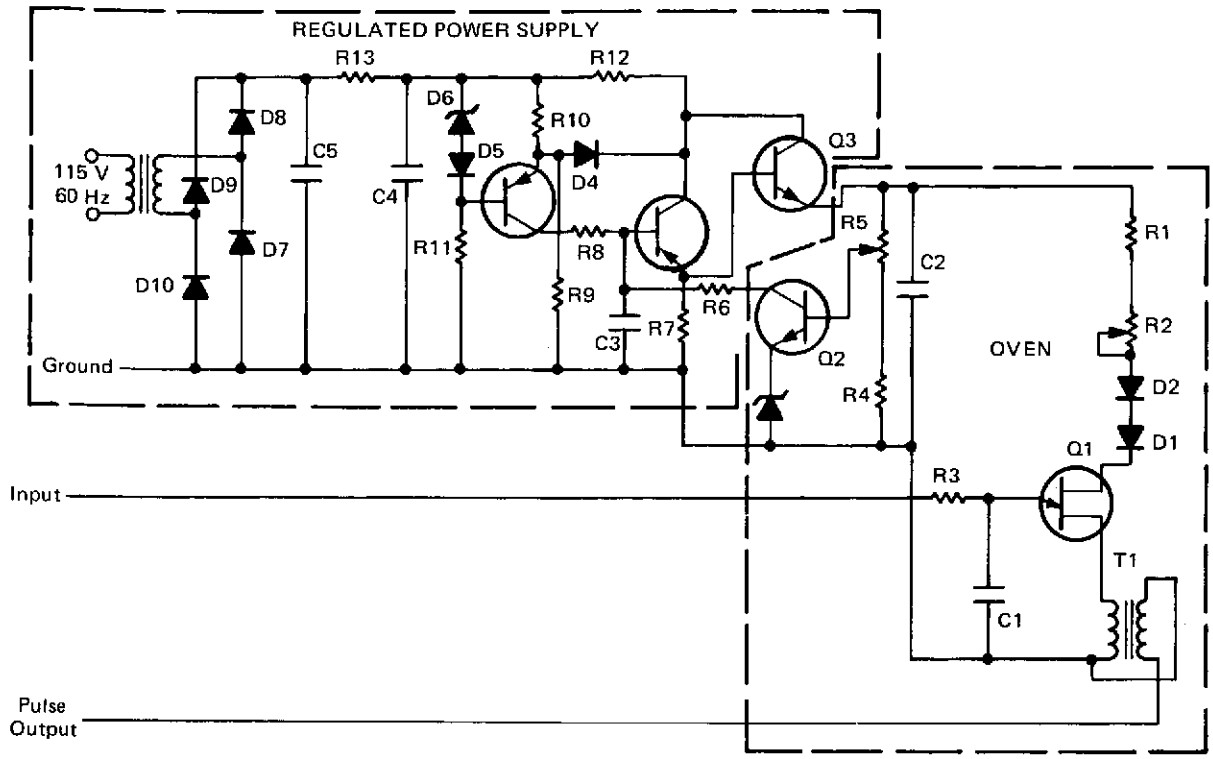
The circuit shown in Figure 1 is a solid-state temperature compensation circuit for power supply output regulation. The circuit consists of an operational amplifier coupled to a resistive feedback network.

When the circuit employs precision resistors, in both the reference and feedback networks, it will yield the output characteristics indicated by the top curve of the coefficient plot (see Figure 2). The addition of resistor R_b to the circuit, the setting of total resistance to the original value of R_a, and the subsequent variation in R_a and R_b will produce an output characteristic virtually unaffected by temperature. The resistor used for R_b must be composition carbon. It is noted that this circuit can be inverted for applications where an excessive positive temperature coefficient is the problem.

Source: R. R. Walker of
Rockwell International Corp.
under contract to
Johnson Space Center
(MSC-17903)

No further documentation is available.

PRECISION VOLTAGE TOLERANCE DETECTOR



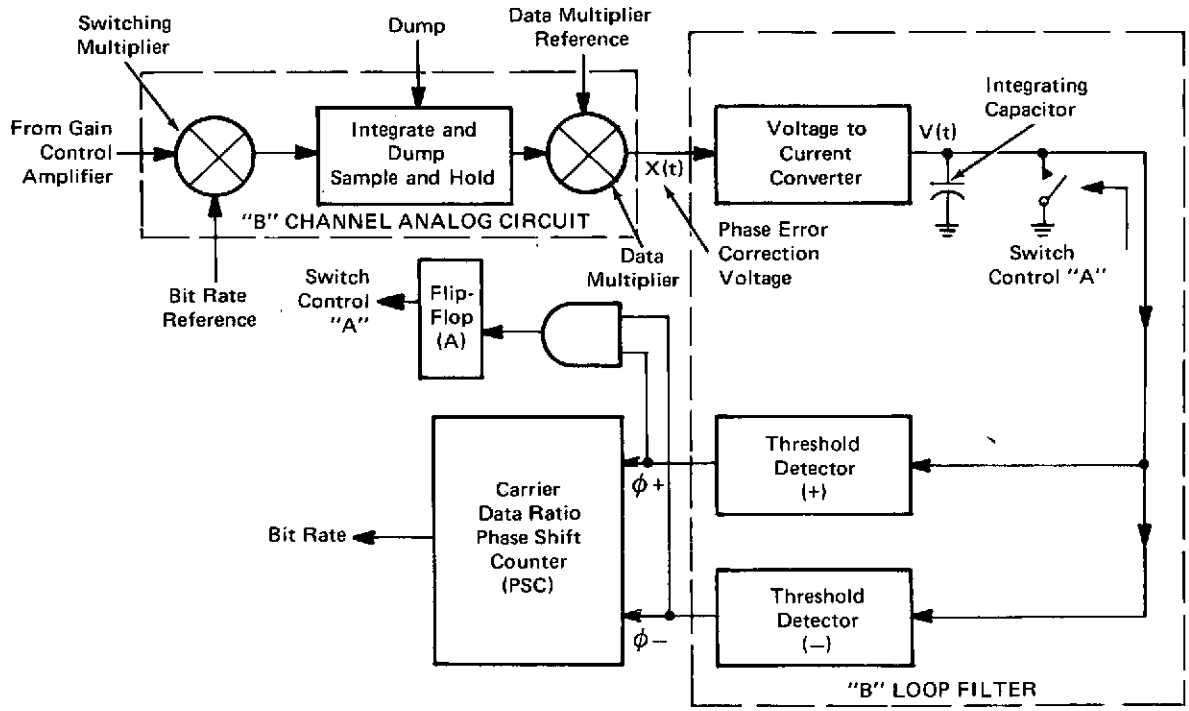
The circuit shown in the figure is a precise fixed reference voltage variation detector. The tolerance detector consists of a unijunction transistor relaxation oscillator trigger circuit and stable power supply with the trigger circuit components and the voltage reference components of the power supply mounted in a single oven for common temperature environment.

When a dc voltage is applied to the input of the circuit, and the voltage is constant, there is no output from the trigger circuit. When the dc voltage that is being monitored by the circuit exceeds the setting for which it is designed (from nine to eleven volts) by one part in 10,000, the trigger circuit starts to generate a pulse train which may be used to display a warning lamp or control a flip-flop input to a system for controlling voltage.

Source: M. F. Hanna of
Caltech/JPL
under contract to
NASA Pasadena Office
(NPO-10676)

Circle 8 on Reader Service Card.

BANG-BANG BIT SYNCHRONIZER LOOP



The function of the bit sync loop in a bit synchronizer is to establish bit time synchronism of a PSK/PCM (phase shift key/pulse code modulation) waveform. After subcarrier phase lock is achieved, the bit sync loop establishes the exact dump time for the integrate-and-dump matched filters by resolving the N - 1 phase lock ambiguities of the subcarrier loop (N = number of subcarrier cycles per bit time). Conventional bit sync loops have in the past achieved this function by either employing an independently controlled voltage controlled oscillator (VCO) loop or by use of a proportionally controlled phase shift counter (PSC) driven by the VCO in the subcarrier loop.

A more effective arrangement has been conceived utilizing the concept of a bang-bang controlled PSC in the bit sync loop. The bang-bang circuit consists of a resettable integrator which precedes a symmetrical, dead-zone, hard-limiter, non-linear device. The main advantage of the bang-bang bit synchronizer loop concept is its simplicity which yields a more reliable and lower power design.

The figure shows the basic configuration of the bit sync loop. The function of this loop is to derive bit phase synchronization. That is, if the signal is biphase modulated onto a subcarrier such that there are carrier data ratio (CDR) subcarrier cycles per bit time, there are 2 CDR possible phase ambiguities which this loop must resolve. This corresponds to establishing the beginning of the bit period at the appropriate half subcarrier cycle. The loop configuration consists of three major elements:

(1) The B channel analog circuitry
(2) The B loop filter
(3) The "bang-bang" controlled CDR phase shift counter.

The function of the B channel circuitry is to derive from the input signal a phase error correction voltage X(t) proportional to phase error ϕ which exists in the loop. In this regard, the switching multiplier circuit first removes the subcarrier modulation, the integrate-and-dump circuit provides a matched filter to the waveform which maximizes the signal-to-noise ratio (SNR), and the data multiplier removes the original non-return-to-zero (NRZ) data from the signal. Hence, the output X(t) of the data multiplier is zero unless a bit phase timing error exists in the loop.

The function of the loop filter is to integrate the error signal X(t) out of the data multiplier to enhance the "error signal-to-noise ratio".

The function of the bang-bang controlled PSC is to respond to the integrated bit synchronizer

loop correction voltage V(t) in the following way. Two threshold detection circuits (in the B Loop Filter) set at $+V_T$ and $-V_T$ volts, respectively, are used to continuously monitor V(t). The bit period is divided into N equal increments by means of a PSC. This PSC is a preset counter which is capable of dividing its input clock by N or N ± 1 during any one given bit period. This is done in accordance with the simple rules in the table.

Table. Rules for Discussion of Input Clock

Integration Voltage V(t)	Division Ratio of Phase Shift Counter	Resultant Phase Error of Bit Synch Loop
$-V_T < V(t) < V_T$	N	Unchanged
$V(t) \leq -V_T$	N−1	Decreased by 1/N of a bit period
$V(t) \geq V_T$	N+1	Increased by 1/N of a bit period

Each time the PSC changes the phase of the loop (i.e., divides by N − 1 or N + 1) a control flip-flop (A) shown in the figure is toggled which discharges the capacitor. This merely insures that the integration voltage V(t) always starts out at zero voltage midway between the two threshold levels + V_T.

Source: B. Dunbridge of
TRW, Inc.
under contract to
Johnson Space Center
(MSC-13264)

No further documentation is available.

Notes: